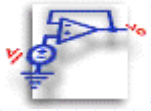

Section 3.3 Application of Surge Arresters

Section 3.3.1 Introduction

A surge arrester is a protective device whose function is to maintain its voltage at a ceiling value below the Basic Insulation Level (BIL) of the equipment it protects. Surge arresters are connected between each phase terminal of the protected equipment and the ground. The protection properties of an arrester are due to the nonlinear characteristic between the arrester voltage and its current.

Abnormal system operation, such as switching, lightning strikes, or temporary reactive power unbalances, will cause surges and/or temporary overvoltages in the system (To learn more about system overvoltages, see **Section 3.1b**). Under these conditions, the surge arrester must conduct a high current which limits the overvoltage at the equipment to levels that are safe for the equipment's insulation. The energy dissipation in the arrester during overvoltage raises the temperature of the arrester. The highest energy dissipation in the arrester occurs during temporary overvoltages, since their duration can approach several hundreds of milliseconds. If this energy exceeds the dissipation capability of the arrester, thermal runaway may occur, which will destroy the arrester.

The correct application of surge arresters in system insulation coordination requires knowledge of the overvoltage in the system as well as the maximum energy the arrester is expected to absorb. This section describes the main characteristics of surge arresters and provides a method for the calculation of arrester energy and system voltage in abnormal system conditions.

Section 3.3.2 Definitions

Insulation coordination is the process of matching the characteristics of the equipment insulation with the characteristics of the protective device (surge arresters). If the insulation coordination is successful, then the probability of insulation failure under expected abnormal system conditions is minimized.

Insulation breakdown is a statistical phenomenon and insulation properties are typically obtained experimentally. In general, these capabilities depend on the crest value and duration of the applied voltage. Insulation can withstand high voltage for short duration. As the applied voltage duration increases, the withstand level of the insulation decreases. The relationship between peak applied voltage and maximum duration before breakdown can be obtained experimentally for various waveforms of applied voltage. This characteristic is called **insulation withstand curve**.

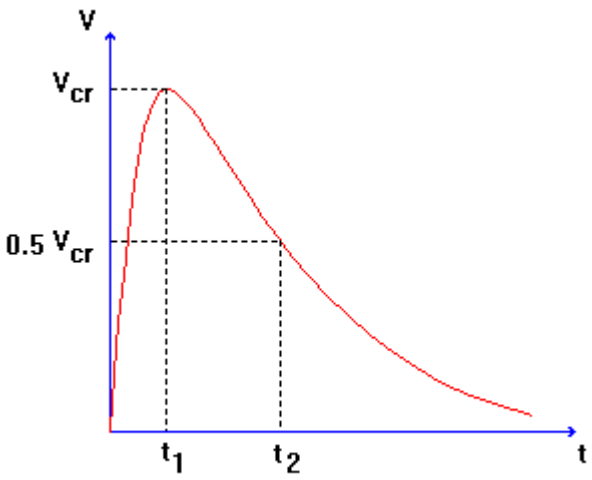

Fig. 3.3.1 Standard impulse waveform

Standard voltage waveforms used to test the insulation capability are called voltage impulses. These waveforms represent the shape of the voltage that occurs during switching and lightning operations. With reference to Figure 3.3.1, an impulse waveform is characterized by its crest or peak value, Vcr, its rise time, t1, and its tail time, t2. The rise time is the time from the impulse application to the impulse crest. The tail time is the time from the impulse crest to half the crest value. A typical impulse waveform is the one with 1.2 μs rise time and 50 μs tail time. This waveform is described as a 1.2×50 μs wave.

Basic insulation level (**BIL**) is the crest of the standard impulse voltage representing the worst case of surge voltage that may appear in the system. BIL depends on the system operating voltage and it is standardized for different operating voltages. For safe operation, the equipment insulation must be capable of withstanding repeated application of standard voltage impulses conforming to the system BIL.

Protection of equipment insulation is achieved by employing surge arresters. For successful protection, the arrester must provide a ceiling voltage that lies under the insulation withstand curve of the equipment. The difference between the insulation withstand voltage and the arrester ceiling voltage is **the protection margin**.

Section 3.3.3 Surge Arrester Characteristics

A surge arrester is a nonlinear resistor. The arrester resistance provides the following properties that are useful for system protection. Its resistance is high under normal system voltage. This high resistance minimizes the steady state losses in the arrester. Its resistance decreases under overvoltage conditions. The decreased resistance provides an alternate discharge path for surge currents and maintains the system voltage under safe values. In addition, the arrester must be capable of dissipating the energy of the surge without damage to itself. If, during overvoltage conditions, the dissipated energy is below the arrester capability, the arrester resistance will return to its high value when the overvoltage conditions are removed from the system. If, however, the energy absorbed by the arrester exceeds its capability, the arrester resistance will maintain its low value even under normal system voltage, resulting in a permanent short-circuit.

There are four classes of arresters, dependent on the voltage and energy ratings of the system. These are, in order of power rating: station arresters, applied at systems operating above 138 kV; intermediate arresters, applied at transmission systems operating below 138 kV; distribution arresters, applied to distribution systems operating above 1000 V; and secondary arresters, applied to systems with voltage below 1000 V.

A surge arrester can be implemented using a combination of gaps and silicon carbide resistors (with the desirable non-linear characteristic). An arrester also may be gapless using stacks of only metal-oxide varistors (MOV's) as the nonlinear element. The parts of the voltage-current characteristic of an MOV consists of the following regions:

a. Leakage region. This is the region in which the arrester operates under normal system voltage. In this region, the MOV draws a current with a density less than 0.1 mA/cm2. The leakage region is characterized by a small nonlinearity.

b. The transition region. This region is where the nonlinear behavior of the material starts. The voltage measured at the material for a current density of 1 mA/cm2 is **the transition voltage**.

c. The highly nonlinear region. This region is characterized by large incremental current changes for small incremental voltage changes.

The leakage region of the MOV is sensitive to the device operating temperature. This region is characterized by a positive thermal coefficient, i.e. a rise in temperature results in higher leakage current. As a result, the dissipation in the material increases. Therefore, thermal runaway is possible, if unfavorable conditions exist.

The discharge voltage in an MOV increases as the rate of change in the discharge current increases. This dielectric property influences the design of MOV-based arresters. The arrester must be able to discharge a standard lightning current (typically 10 kA crest) under a discharge voltage that is considerably below the BIL.

To construct a surge arrester, MOV disks are stacked into a column. The number of disks in the column is determined by the dielectric properties of the disks, such that the resulting discharge voltage provides the required protection margin for the equipment insulation. An arrester may consist of more than one column. The number of columns is predominantly determined by the energy requirements of the arrester. The energy capability of an arrester column is calculated by multiplying the energy capability of each disk (provided by the manufacturer) by the number of disks per column. From simulation studies, the energy requirements of the arrester are calculated. Then, the number of columns is decided to match these requirements.

Arrester V-I Characteristic

The V-I characteristic of an arrester can be found from the V-I characteristic of the arrester disks by combining all disks in a column in series, and all columns in parallel.

Consider an arrester disk with the following parameters:

Disk diameter:

$D := 50\ cm^2$

Disk thickness:

$h := 2.1\ cm$

DC voltage at 1 mA/cm2:

$E := 1640\ \frac{V}{cm}$

DC leakage current density at 80% of DC voltage at 1 mA/cm2:

$J := 2\ \frac{A}{cm^2} \cdot 10^{-6}$

Voltage ratio V@300 A/cm2 / V@1 mA/cm2:

$V300\_1 := 1.70$

The arrester V-I characteristic is given by Equation (3.3.1).

$$I(V) = p \cdot \left(\frac{|V|}{Vo}\right)^{\alpha} \cdot sgn(V) \qquad \textbf{(3.3.1)}$$

where

I is the discharge current of the arrester,

V is the discharge voltage of the arrester, and

Vo is the transition voltage of the arrester.

α describes the sharpness of the nonlinear region of the arrester. This parameter is typically between 10 and 50.

p is adjusted to provide the leakage current of the arrester under normal voltage conditions.

The parameters in Equation (3.3.1) are found from the manufacturer's as follows:

The parameter, Vo, is calculated from the disk thickness and the dc voltage at 1 mA/cm2.

$Vo := h \cdot E \qquad Vo = \left(3.444 \cdot 10^3\right)\ V$

The alpha of the arrester is calculated from V300_1 by using Equation (3.2.1). Therefore, we have

$$\frac{300\ A}{1\ m \cdot A} = \left(\frac{V300}{V1}\right)^{\alpha} = V300\_1^{\alpha} \qquad \text{and} \qquad \alpha := \frac{\ln\left(\frac{300\ A}{1 \cdot 10^{-3}\ A}\right)}{\ln(V300\_1)} = 23.767$$

Parameter, p, is found from the disk diameter and J. Therefore, using Equation (3.2.1) we have

$$J \cdot D = p \cdot 0.8^{\alpha} \qquad \text{from which} \qquad p := \frac{J \cdot D}{0.8^{\alpha}} = 0.02\ A$$

If the arrester is going to be applied on a 138 kV system, the number of disks, n, must be such that the peak steady state leakage current does not exceed 1 mA/cm2. Typically, the transition voltage of the arrester is 1.5 times higher than the normal line to neutral peak voltage (for a line to neutral application). Therefore,

$$n := \text{ceil}\left(\frac{\sqrt{\frac{2}{3}} \cdot 138 \cdot 10^{3} \cdot 1.5\ V}{E \cdot h}\right) = 50$$

To obtain the combined characteristic, Vo calculated above must be multiplied by n.

$$Vo := n \cdot Vo = \left(1.722 \cdot 10^{5}\right)\ V$$

If more than one column is used, the parameter, p, must be multiplied by the number of parallel columns. The combined arrester characteristic for one column is shown below.

$$V := -1.4 \cdot Vo, -1.35 \cdot Vo .. 1.4 \cdot Vo \qquad sgn(x) := \text{if}\ \langle x > 0, 1, -1 \rangle$$

$$I(V) := p \cdot \left(\frac{|V|}{Vo}\right)^{\alpha} \cdot sgn\left(\frac{V}{V}\right)$$

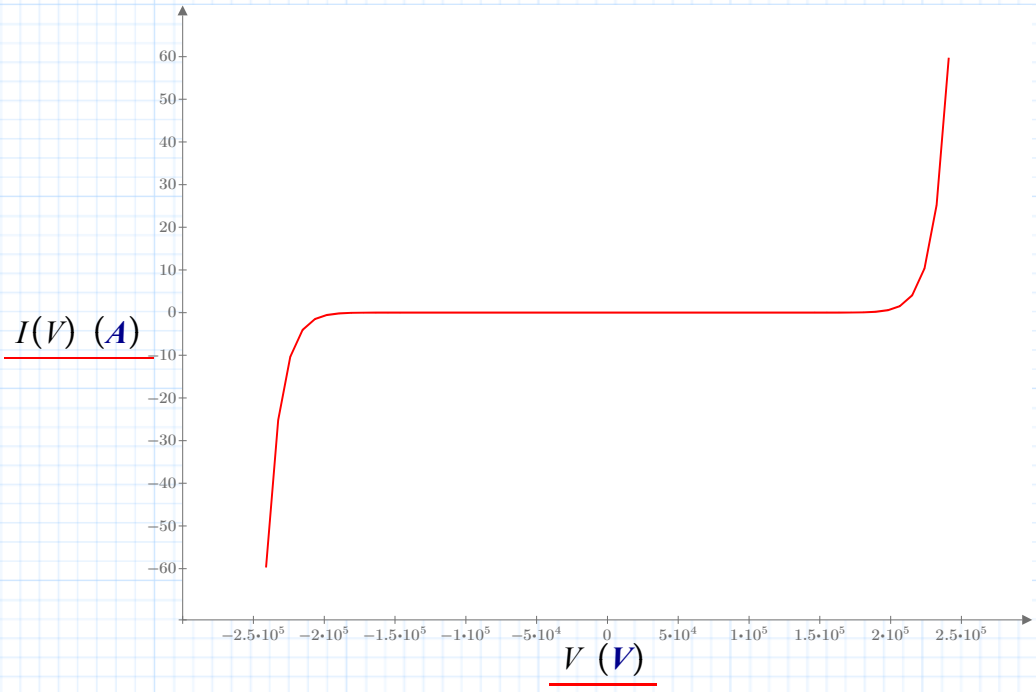

Fig. 3.3.2 Arrester V-I characteristic

Section 3.3.4 Energy Calculations

The conditions which stress the arrester dissipation capacity are reactive power unbalances near the arrester. These unbalances cause temporary overvoltages of long duration. Also, other types of slow transients have considerable effect on the energy dissipation, such as harmonic overvoltages and transient overvoltages in transformer energization. The arrester energy is calculated for the worst case scenario by performing a system simulation.

Consider the single-phase system of Figure 3.3.2, where the above calculated arrester column is applied between the bus and the ground. The capacitance may correspond to load compensation. The following example shows the arrester response under a no-load bus energization. In a practical application problem, the transformer saturation also must be included, since it will influence the system response.

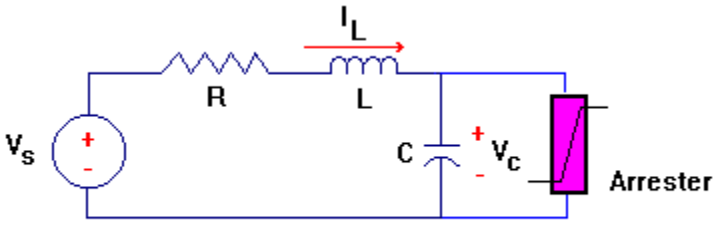

Fig. 3.3.3 Application example

The system parameters are

$R := 3.5\ \Omega$

$L := 35 \cdot 10^{-3}\ H$

$C := 70 \cdot 10^{-6}\ F$

$Vs(t) := \sqrt{\frac{2}{3}} \cdot 138 \cdot 10^{3}\ V \cdot \cos(\omega \cdot t + \phi)$

$\omega \equiv 377\ \frac{rad}{s}$ $\qquad \phi \equiv 10\ deg$

The breaker recloses at t = 0. Following the analysis presented in Section 3.1, the system dynamic equations are

$DI(I_L, V, t) := \frac{Vs(t) - V - R \cdot I_L}{L}$ current derivative

$DV(I_L, V, t) := \frac{I_L - I(V)}{C}$ voltage derivative

Define time step for solution.

$dt := 0.1\ \textbf{\textit{ms}}$

Define solution duration.

$T := 100\ \textbf{\textit{ms}}$

Define required solution points.

$N := \frac{T}{dt}$

Define initial conditions.

$I_{L_0} := 0\ \textbf{\textit{A}}$ $\quad I_{L_1} := I_{L_0}$

$V_0 := 0\ \textbf{\textit{V}}$ $\quad V_1 := V_0$

$E_0 := 0\ \textbf{\textit{J}}$ arrester energy

$E_1 := E_0$

Define auxiliary constants.

$h1 := 1.5 \cdot dt$ $\quad h2 := 0.5 \cdot dt$

Perform numerical solution.

$i := 1 .. N$ $\quad t_i := i \cdot dt$

$$\begin{bmatrix} I_{L_{i+1}} \\ V_{i+1} \\ E_{i+1} \end{bmatrix} := \begin{bmatrix} I_{L_i} + h1 \cdot DI\left(I_{L_i}, V_i, t_i\right) - h2 \cdot DI\left(I_{L_{i-1}}, V_{i-1}, t_{i-1}\right) \\ V_i + h1 \cdot DV\left(I_{L_i}, V_i, t_i\right) - h2 \cdot DV\left(I_{L_{i-1}}, V_{i-1}, t_{i-1}\right) \\ E_i + V_i \cdot I\left(V_i\right) \cdot dt \end{bmatrix}$$

The arrester voltage is

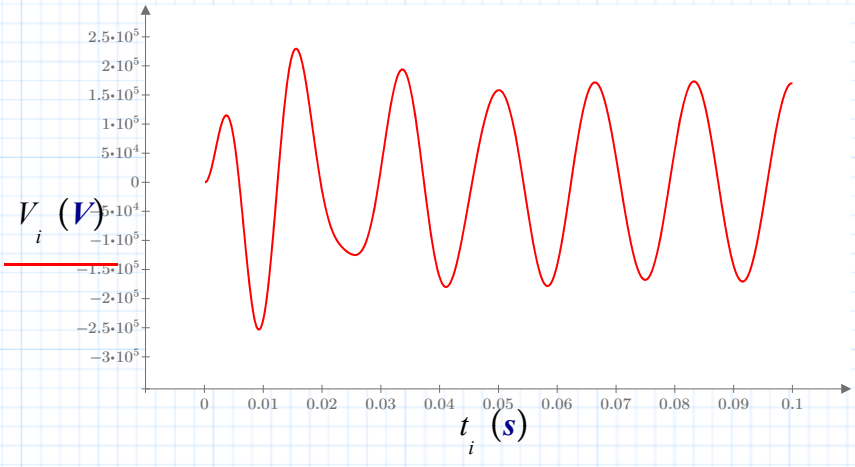

Fig. 3.3.4 Voltage across arrester

The arrester current is

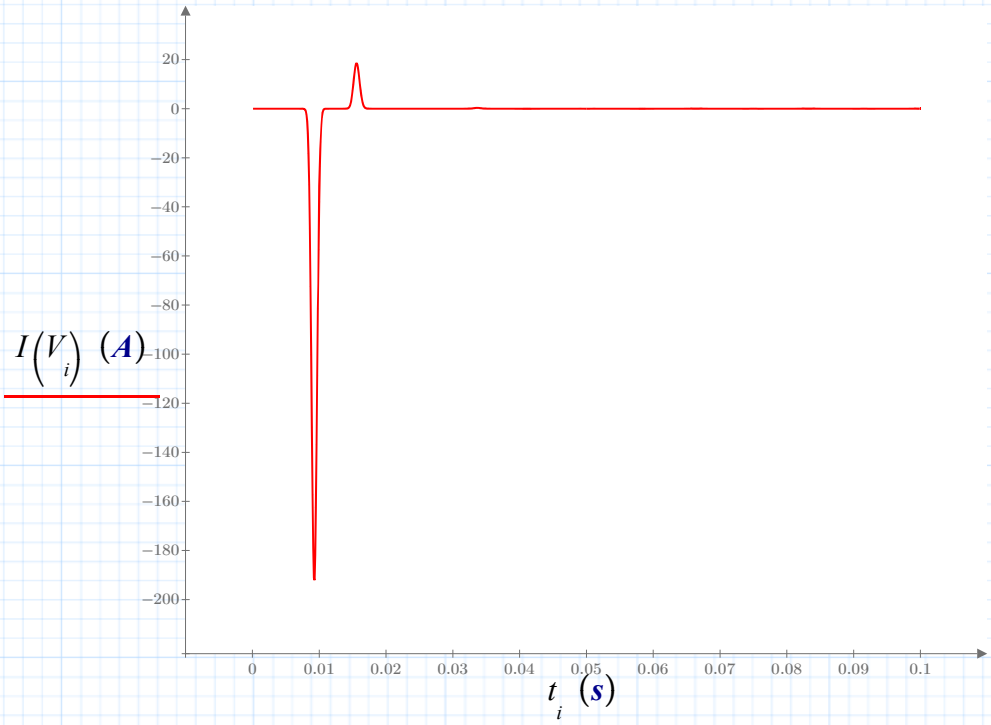

Fig. 3.3.5 Arrester discharge current

The energy dissipated in the arrester as function of time is

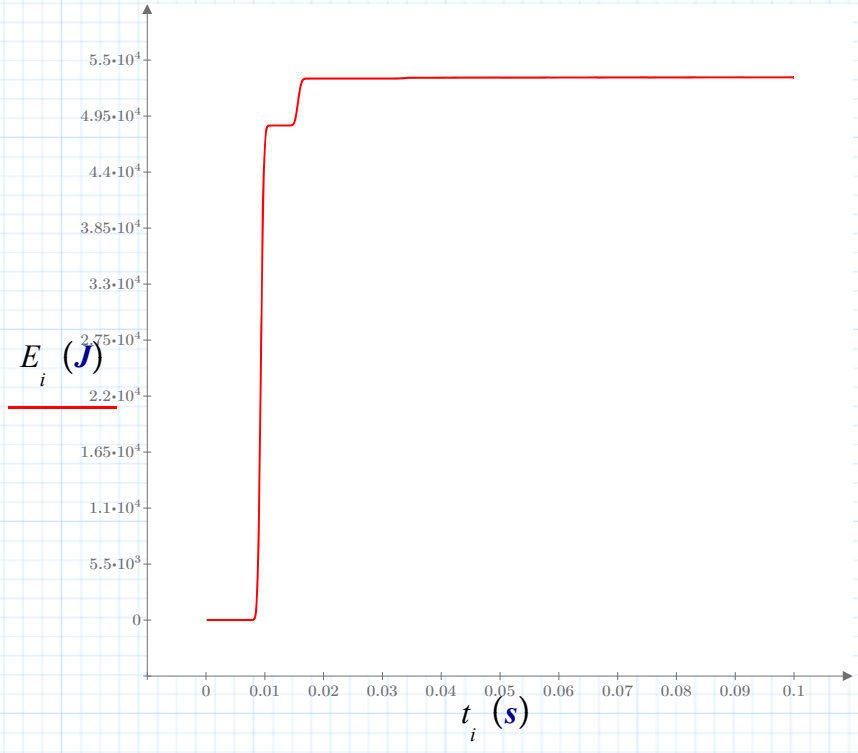

Fig. 3.3.6 Arrester energy dissipation

From the above graph, the arrester must dissipate 55 kJoules of energy during this transient.