energy/transition, delay, power density, and compute density, taking into account only high-performance CMOS. It can be seen that crossbar-based circuits show clear potential for superiority in area, as well as in energy consumption, but not yet in performance. Furthermore, as long as the cost of building CMOS chips continues to follow an exponential law with time, it is pointed out that it is reasonable to expect that molecular chips will be less expensive to build, since chemical self-assembly is used to build the devices, rather than many, very precise lithography steps.

Moreover, Jo *et al.* [13] investigate two terminal amorphous-Silicon (a-Si) based resistive switches. These devices are found to exhibit a number of desirable performance metrics in terms of speed (<50 ns programming time), and endurance (>10^5 cycles), which make them suitable for high-performance memory and logic applications based on conventional or emerging hybrid nano/CMOS architectures. Kim *et al.* in [14] demonstrate a high-density, fully-operational hybrid crossbar/CMOS system which utilizes a memristor-based crossbar array. The structure of the studied device consists of an a-Si layer acting as the switching medium. A 50 nm half pitch was achieved through electron beam lithography and yielded an equivalent data storage density of 10 Gbits/cm^2 when storing one bit per memory cell. In addition, Lu *et al.* in [15] review the recent progress on the development of two terminal resistive devices and report on a number of promising performance metrics shown by devices based on solid state electrolytes like a-Si. Specifically, resistance switching speed of < 10 ns and endurance of > 10^8 cycles are mentioned, whereas data retention of >10 years at 85 °C and nominal energy consumption per operation in the subpicojoule range have also been reported [16-19]. Some of the recent advances of binary metal–oxide resistive switching devices reported in the literature are summarized in Table 4 of [20].

Also, Ebong and Mazumder [21] analyze the feasibility of memristor memories and introduce an adaptive read, write, and erase method. The power metrics are compared to flash memory technology, and the memristor-based memory exhibits an energy per bit consumption about one tenth of that of flash when programming, comparable to flash when erasing, and about one fourth of flash when reading. The aforementioned results are summarized in Table I of [21]. Also, Eshraghian *et al.* in [22] provide a new approach towards the design and modeling of memristor-based content addressable memory (CAM). Emerging memory devices and technologies are discussed, and a range of performance parameters and salient features of characteristic emerging technologies for memories can be found in Table II of [22]. The memristor-based crossbar architecture is shown to be highly scalable [23] and promising for ultra-high density memories [24]. It is worth to mention that a memristor with minimum feature sizes of 10 and 3 nm yields 250 Gb/cm^2 and 2.5Tb/cm^2, respectively.

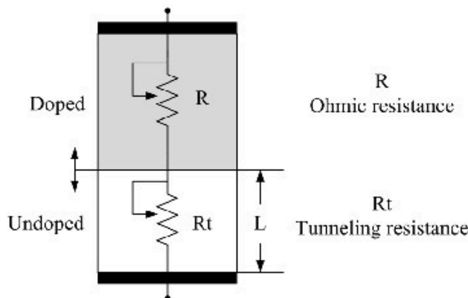

Fig. 1. Equivalent circuit of the coupled ohmic-tunneling variable-resistor model; L is the width of undoped dioxide layer (tunnel barrier width).

It is worth to mention that in 2010, almost two years after their first memristor announcement (their device comprised a 50 nm titanium dioxide film and exhibited ion mobility of 10^{-10} cm^2/(Vs)), HP Labs also declared that they had practical memristors working at 1 ns (~1 GHz) switching times and 3 nm by 3 nm sizes, with an impressive electron/hole mobility of 1 m/s [25]. These statistics forespeak well for the future of the technology and memristors could easily rival the current sub-25 nm flash memory technology.

III. Memristor Device Modeling

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A. Related Work

The HP Laboratories group in their first memristor implementation announcement [3], along with experimental device examples, suggested a coupled variable-resistor model for memristors. Ever since, this model was improved by Joklegar and Wolf [26], whereas several papers by HP [27], [28] report on further developments of resistance switching theory for T_iO_2 devices. Di Ventra *et al.* [29] suggested a simple threshold-type model of memristive systems [30] and employed it in programmable analog circuits [31], [32]. Liu *et al.* [33] proposed a material-oriented methodology to control resistance switching behavior of oxide-based resistive switches, based on a unified physical model [34] where formation of conducting filaments (CFs) is due to the generation of new oxygen vacancies by ionizing oxygen ions from the lattice under voltage bias. Furthermore, approximated SPICE memristor models have been proposed and tested with promising simulation results [35]. However, little work has been done towards memristor modeling, whereas various implementation paradigms are continually being proposed combining nano/CMOS [7], reconfigurable architectures and memristors [36], [37], resulting in hybrid implementations [38], [39], that could have a profound effect on integrated circuit performance.

B. A Novel Memristor Circuit Model

We propose an alternative solution for modeling memristors, explaining the devices memristive behavior by investigating the occurrence of quantum tunneling [9]. The equivalent circuit of the proposed model is depicted in Fig. 1. It is a threshold-type switching model of a two-terminal voltage-controlled electrical device that exhibits memristive behavior [30], and it is described by the following expressions:

$$I(t) = G(L,t)V_M(t) \tag{1}$$

$$\dot{L} = f(V_M, t). \tag{2}$$

L is the single state variable of the system which in our model

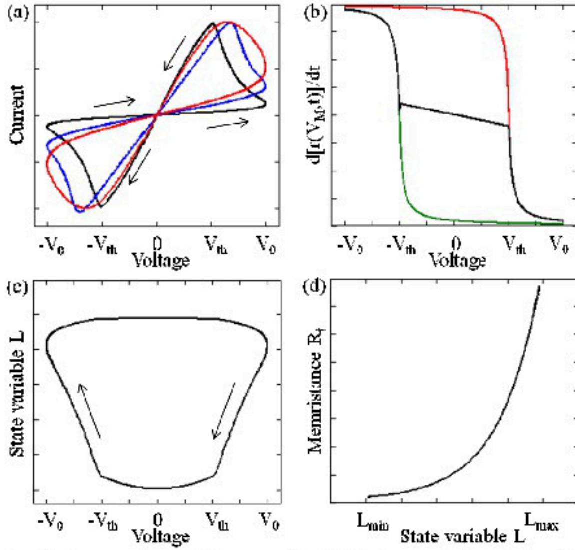

Fig. 2. (a) A comparison of the normalized I-V characteristics obtained from a memristor under ac voltage given by the equation $V(t)=V_0\sin(\omega t)$, with V_0=4V and threshold voltage V_{th}=2V. The models' results are from: the proposed model (black), the model in [3] including a proposed modified window function from [26] (blue), and the model in [29] (red). (b) Graphical representation of (6). In the region [$-V_0$,$-V_{th}$) the graph (black) follows the green sigmoid function, whereas in the region (V_{th}, V_0] it follows the red one. (c) Response of the state variable L according to (5), and (d) the device memristance R_t given by (4) for a restricted range of the state variable L.

is the tunnel barrier width (thickness of the free of oxygen vacancies dioxide layer), with the electrical current transport process being limited primarily by tunneling through it. Also, G is the device's conductance and V_M is the applied ac voltage. The time derivative of the state variable in (2) is interpreted as the speed of movement of the barrier between the two layers, due to the applied voltage bias.

We suggest the coupled ohmic-tunneling variable-resistor equivalent circuit of Fig. 1, where we consider an ohmic variable-resistor R and a tunneling variable-resistor Rt connected in series. R represents the resistance of the doped dioxide layer and Rt represents the tunneling resistance of the undoped layer of the device. The doped layer acts as a conductor, whereas the undoped layer is a pure insulator. There is therefore a significant difference between the actual values of their resistances, with $Rt >> R$, which is the reason why our proposed model concentrates mainly on the Rt.

Tunneling resistance Rt is expected to be proportional to the tunnel barrier width L, given the fact that the larger the barrier width, the higher the resulting resistance should be. Also, its value is anticipated to change according to the movement of the boundary between the two materials because of the transport of oxygen deficiencies under positive or negative sinusoidal voltage. Thus, any mathematical formulation for Rt could include at least a fitting parameter which would bound the effect of the device's varying geometry on the actual concentration of the oxygen vacancies in either of the sides (doped/undoped) of the T_iO_2 film. Furthermore, according to Schiff [9], Rt is inversely proportional to the product of the voltage-dependent tunneling transmission coefficient, denoted here as T_0, and the electron effective density of states, defined here as N_{eff}, whereas it is exponentially proportional to the tunnel barrier width L. Therefore, its particular mathematical formulation is:

$$Rt\,(V_M) = \frac{1}{N_{eff}} \cdot \frac{e^{2k_{V_M}L}}{T_{0,V_M}}. \tag{3}$$

The voltage dependence of (3), due to the presence of the voltage-dependent parameters T_0 and k, can be translated into a corresponding variation of the tunnel barrier width L; therefore it can be passed to a new voltage-dependent parameter $L_{VM,t}$ with no significant error implication. In our model, we defined Rt to be described by the following equation, whose graphical representation is demonstrated in Fig. 2(d):

$$Rt\,(L_{V_M,t}) = f_0 \cdot \frac{e^{2L_{V_M,t}}}{L_{V_M,t}}. \tag{4}$$

Equation (4) gives the devices resistance (memristance) for a certain restricted range of the state variable L. All unknown material-specific and geometrical issues are contained into the model-fitting constant parameter f_0, whose value has been determined by comparison with experimental results [3]. The qualitative agreement of (3) and (4) verifies our assumption for the exponential dependence of the tunneling resistance on the tunnel barrier width.

In addition, the tunnel barrier width is expected to vary within a restricted valid range, based on the assumption that the switching rate of L is small (fast) below (above) a threshold voltage V_{th}. A heuristic equation $L(V_M, t)$ that qualitatively gives the expected response of the tunnel barrier width as a function of time t and applied voltage V_M is given below, whereas the corresponding graph is shown in Fig. 2(c):

$$L\,(V_M, t) = L_0 \cdot \left(1 - \frac{m}{r(V_M, t)}\right). \tag{5}$$

L_0 is the maximum value that L can attain. The term in parenthesis of (5), which contains a voltage-dependent function $r(V_M, t)$ and a fitting constant parameter m, determines the boundaries of the barrier width. The function $r(V_M, t)$, incorporates the assumption for the expected different switching rate of L based on the applied voltage bias discussed above. Particularly, the time derivative of $r(V_M, t)$ is given by the following equation:

$$\dot{r}(V_M, t) = \begin{cases} a \cdot \dfrac{V_M + V_{th}}{c + |V_M + V_{th}|}, & V_M \in [-V_0, -V_{th}) \\ b \cdot V_M, & V_M \in [-V_{th}, +V_{th}] \\ a \cdot \dfrac{V_M - V_{th}}{c + |V_M - V_{th}|}, & V_M \in (+V_{th}, +V_0] \end{cases}. \tag{6}$$

Equation (6) comprises one-parameter sigmoid functions for

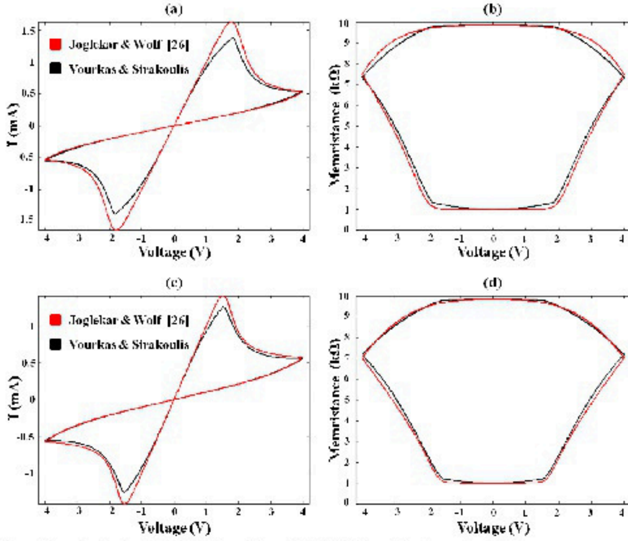

Fig. 3. Calculated *I-V* (a, c) and *M-V* (b, d) characteristic responses of memristors with $L_{0,1}$ = 3nm and $L_{0,2}$ = 5nm, for a 8V peak-to-peak triangular voltage pulse of period T_1=2.6 s and T_2=5.5 s, respectively, according to the presented here model and the model of Joglekar & Wolf [26]. Our model successfully reproduces the characteristic responses by setting $\{a, b, c, f_0, m, |V_{th}|\}$ to the values {1000, 50, 0.1, 86.49, 56.06, 1.7V} and {350, 20, 0.1, 2.67, 29.97, 1.5V}, correspondingly.

the regions above V_{th} (first and last leg), whereas a linear relation of the applied voltage is used for the region below V_{th}. a, b, and c are fitting constants that define the slope and the magnitude of (6), with $a>>b$ and $0<c<1$. A different set of values for the parameters $\{a, b, c, m\}$ defines a different set of boundaries for the tunnel barrier width in (5). The graphical representation of (6) is shown in Fig. 2(b), where the two sigmoid functions were also included separately to facilitate visual correspondence. It is obvious that in the region $[-V_0, V_{th})$ the graph (black line) follows the green sigmoid graph, whereas in the region $(V_{th}, V_0]$ follows the red graph. Equations (5) and (6) bound the fundamental switching dynamics in TiO_2-based memristive devices, correlating the tunnel barrier width L with the applied voltage V_M.

C. Verification of the Proposed Model

Fig. 2(a) demonstrates a comparison of the normalized *I-V* hysteretic curves obtained from a memristor under ac voltage bias, between our model and two published device models [26], [29]. The results of our model exhibit the expected “bow tie” shape, and apparently correspond qualitatively to the other models’ simulation results, as well as to the experimental *I-V* curve shown in [3]. In order to illustrate the versatility of our model, we present in Fig. 3 the *I-V* and *M-V* (*M*-Memristance) characteristics as calculated by the presented here model and the model proposed by Joglekar and Wolf [26] This model is an extension of the linear ionic drift as described by HP [3], where a particular window function is incorporated to illustrate nonlinearities in ionic transport. In order to obtain a fairer comparison, where it applies we use the same parameters for both models. In specific, we use an 8V peak-to-peak triangular voltage pulse of period T_1=2.6 s and T_2=5.5 s to simulate memristors with total width $L_{0,1}$ = 3nm and $L_{0,2}$ = 5nm, respectively. We consider a R_{off} / R_{on} ratio of ~10, a dopant mobility of $3x10^{-8}$ $m^2/(Vs)$ [22] and we set the exponent variable of the corresponding window function p=2 [26]. Fig. 3 summarizes the simulation results for both the first (a, b) and the second (c, d) memristor. In each simulation we set our model’s parameters $\{a, b, c, f_0, m, |V_{th}|\}$ to the values {1000, 50, 0.1, 86.49, 56.06, 1.7V} and {350, 20, 0.1, 2.67, 29.97, 1.5V}, respectively. In both cases our model delivers satisfying quantitative results which coincide with the results from the published model. The small difference in the maximum observed currents is attributed to the slightly different moments when the maximum memristance is achieved, particularly shown in Fig. 3 b, d.

Moreover, Pickett *et al.* in [40] report on experimental results from the application of a dynamical testing protocol applied to a set of TiO_2-based memristive devices. Through analysis of the switching dynamics that arise from ionic motion in the devices, it is concluded that electronic conduction in these devices is dominated by an effective tunneling barrier width that varies with time under the applied voltage. Thus, the switching effect is primarily attributed to an effective tunneling distance modulation, which supports our initial assumptions. Therefore, although the switching behavior is definitely complex, it has been showed that it is well represented in our model. Compared to other published models, like the HP’s model [3], our proposed model provides intuition into these strongly nonlinear dynamical systems, comprising simple and well understood equations and avoiding the use of restrictive material-specific parameters [3], [40]. Different value-sets for all fitting parameters, namely $\{a, b, c, f_0, m\}$, provide the capability of simulating TiO_2-based memristive devices with different physical structures and geometries. In addition, our model offers the option for different threshold voltages to be applied to the ON and OFF switching cases respectively, in order to simulate asymmetric dynamical behavior during each case. Although symmetric behavior is presented here as the default option, various tunneling distance change rates could be attributed to the interaction of the external applied field, the internal field of the concentrated vacancies, and the diffusion, all acting in the same or in the opposite directions according to the applied voltage bias [40].